

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 – 12 (Deleted)

13. (Currently Amended) An integrated circuit package comprising:

- (a) a substrate devoid of horizontal traces, said substrate having terminal pads arranged ~~in at least one row~~ along a perimeter of a surface of said substrate;
- (b) electrically conductive vias ~~holes~~ connecting said terminal pads directly to connectors aligned with the terminal pads on an opposite side of said substrate;
- (c) a semiconductor chip mounted on the substrate, inside said perimeter, said chip having bond pads located on a surface of said chip; and
- (d) a plurality of insulated bond wires, each of said bond wires extending from a bond pad on said chip to a terminal pad on said substrate, ~~said substrate being sized and shaped to provide a sufficient number of rows of terminal pads and associated said via holes so that horizontal traces through said substrate are not required.~~

14. (Original) An integrated circuit package as claimed in claim 13, wherein said substrate is configured to contain a minimal number of layers, to reduce interlayer inductance, capacitance, and cross talk, and to increase the range of bandwidth performance.

15. (Original) An integrated circuit package as claimed in claim 14, wherein said substrate is a single layer substrate.

16. (Original) An integrated circuit package as claimed in claim 14, wherein said substrate contains no lead frames.

17. (Original) An integrated circuit package as claimed in claim 16, wherein said opposite side of said substrate contains a ball grid array, and each of said terminal pads connects to a ball in said ball grid array through said via directly traversing said substrate.

18. (Original) An integrated circuit package as claimed in claim 13, wherein said insulated bond wires extending between said bond pads on said chip and said terminal pads on said substrate are positioned to reduce parallelism between adjacent wires, to in turn reduce cross talk and increase the range of bandwidth performance.

19. (Original) An integrated circuit package as claimed in claim 18, wherein said insulated bond wires are attached in a generally X or Y shaped pattern.

20. (Original) An integrated circuit package as claimed in claim 19, wherein said generally X or Y shaped pattern is an in line or staggered X-Y grid pattern.

21. (Original) An integrated circuit package as claimed in claim 13, wherein at least one of said bond pads is located in an interior portion of said surface of said chip.

22. (Original) An integrated circuit package as claimed in claim 21, wherein said bond pad located in said interior portion is electrically connected to one of a power connection and a ground connection on said chip.

23 – 25 (Deleted)

26. (New) An integrated circuit package comprising:

a substrate element having first and second opposed surfaces;

a plurality of terminal pads disposed on a peripheral portion of the first opposed surface
and a plurality of connectors disposed on a peripheral portion of the second opposed surface to define an array of pairs;

each pair comprising a terminal pad and a connector in alignment with one another, and
an electrically conducting via interconnecting the terminal pad to the connector, the
electrically conducting via comprising a pair of straight walls interconnecting the first
and second opposed surfaces;

a semiconductor chip mounted in a central portion of the first opposed surface, the
semiconductor chip comprising a plurality of bond pads on a surface thereof; and

a plurality of bond wires, each bond wire interconnecting a bond pad on the

semiconductor chip to a terminal pad on the substrate element.

27. (New) An integrated circuit package as claimed in claim 26, wherein said substrate is configured to contain a minimal number of layers, to reduce interlayer inductance, capacitance, and cross talk, and to increase the range of bandwidth performance.
28. (New) An integrated circuit package as claimed in claim 27, wherein said substrate is a single layer substrate.
29. (New) An integrated circuit package as claimed in claim 27, wherein said substrate contains no lead frames.
30. (New) An integrated circuit package as claimed in claim 29, wherein said second opposed surface of said substrate contains a ball grid array, and each of said terminal pads connects to a ball in said ball grid array through said via directly traversing said substrate.
31. (New) An integrated circuit package as claimed in claim 26, wherein said insulated bond wires extending between said bond pads on said chip and said terminal pads on said substrate are positioned to reduce parallelism between adjacent wires, to in turn reduce cross talk and increase the range of bandwidth performance.
32. (New) An integrated circuit package as claimed in claim 31, wherein said insulated bond wires are attached in a generally X or Y shaped pattern.
33. (New) An integrated circuit package as claimed in claim 32, wherein said generally X or Y shaped pattern is an in line or staggered X-Y grid pattern.
34. (New) An integrated circuit package as claimed in claim 26, wherein at least one of said bond pads is located in an interior portion of said surface of said chip.
35. (New) An integrated circuit package as claimed in claim 34, wherein said bond pad located in said interior portion is electrically connected to one of a power connection and a ground connection on said chip.